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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/427,300	10/26/1999	TOM Q WELLBAUM	296	2979

7590 02/12/2003

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EXAMINER
PHAN, TRI H

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/427,300	WELLBAUM ET AL.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

2. The attempt to incorporate subject matter into this application by reference to "A SWITCH MATRIX ARCHITECTURE AND TECHNIQUES FOR IMPLEMENTING RAPID HITLESS SWITCHOVER" is improper because the US Patent Application Numbers and the filing dates are missing.

3. The disclosure ("Background of the invention") is objected to because of the following informalities:

- On page 2, lines 16-17 and 20, the phrase "Fig. 3" should be correct to the phrase --- Fig. 2 ---.

- On page 2, line 21, the phrase "Fig. 4" should be correct to the phrase --- Fig. 3 ---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4 and 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim 4 recites the limitations "said first memory" in line 4-5 and "said second memory" in line 8. There is insufficient antecedent basis for these limitations in the claim 4, nor in the parent claims (Claims 1 and 3).

Similar problem exists in Claim 7, lines 4-5 and 8.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Helton et al.** (U.S.5,416,772) in view of **Fukunaga et al.** (U.S.6,118,795).

- In regard to claims 1, 13 and 22, **Helton** discloses *a network element comprises an input circuit configured to receive a first plurality of optical signals* (input optical interfaces 111-113; For example see Fig. 1; Col. 2, Lines 42-63) *being grouped into a plurality of time slots except sequence of the plurality of concatenated time slots being non-conforming with the SONET*

standard (For example see Abstract; Col. 1, Lines 20-37; Col. 2, Lines 5-20; Col. 8, Lines 48-56; wherein data is grouped into designated sequencing time slots, frames and super frames by using the sequencer 510 as specified in details of Fig. 7; Col. 7, Line 27 through Col. 8, Line 14) *and conforming to a synchronous optical network standard* (SONET; For example see Col. 10, Lines 54-56; wherein the standard is defined in Col. 1, Lines 12-42), *a switch circuit coupled to the input circuit and being configured to receive data from the input circuit corresponding to the optical signals* (time multiplex switch; For example see Fig. 1; Col. 2, Lines 42-63) *and an output circuit coupled to the switch circuit for receiving the data and outputting a second plurality of optical signals in response to the first plurality of optical signals* (output optical interfaces 116-118; For example see Fig. 1; Col. 2, Lines 42-63). **Helton** does discloses about the sequencing time slots as specified in Col. 2, Lines 64-68; Col. 5, Lines 2-5; but fails to disclose *selected ones of the plurality of time slots being concatenated, except a sequence of the plurality of concatenated time slots being non-conforming with the SONET standard.* However, such implementation is known in the art.

For example, **Fukunaga** discloses the method of *selecting time slots being concatenated* (For example see Col. 2, Lines 40-44; Col. 4, Lines 10-34; Col. 7, Lines 37-46; wherein, by using the reception and transmission pointer processing section for receiving and setting the concatenation, and the multiplexing section for multiplexing into group in TDM as specified in Col. 14, Lines 14-38).

Helton also fails to disclose the method of *determining a pointer in each of the concatenated time slots and outputting said plurality of concatenated time slots in accordance with the pointer in each of concatenated time slots.*

Fukunaga discloses the method of *determining a pointer in each of the concatenated time slots* (pointer processing section for setting the concatenation; For example see Col. 2, Lines 5-44) *and outputting said plurality of concatenated time slots in accordance with the pointer in each of concatenated time slots* (For example see Col. 5, Lines 5-10).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of the method of *selecting time slots being concatenated and determining a pointer in each of the concatenated time slots and outputting said plurality of concatenated time slots in accordance with the pointer in each of concatenated time slots* by using the pointer processing as taught by **Fukunaga** in **Helton**'s system with the motivation being to improve the ability to concatenate the data signal in SONET system.

- Regarding claims 2, 14 and 16-17, **Helton** further fails to disclose *a pointer determining circuit configures to provide a pointer identification for each of the plurality of concatenated time slots for the output in accordance with the pointer identification.* However, such implementation is known in the art.

For example, **Fukunaga** discloses *a pointer determining circuit* (pointer processing section for setting the concatenation; For example see Col. 2, Lines 5-44) *configures to provide a pointer identification* (concatenation indication; For example see Col. 4, Lines 10-32) *for each of the plurality of concatenated time slots for the output in accordance with the pointer identification* (For example see Col. 5, Lines 5-10).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of *the pointer determining circuit configures to provide a pointer identification for each of the plurality of concatenated time slots for the output in accordance with the pointer identification* by using the pointer processing section as taught by **Fukunaga** in **Helton**'s system with the motivation being to improve the ability to concatenate the data signal in SONET system.

- In regard to claims 3 and 15, **Helton** further fails to disclose *a memory coupled to the pointer determining circuit contains information identifying the plurality of concatenated time slots.* However, such implementation is known in the art.

For example, **Fukunaga** discloses *a memory coupled to the pointer determining circuit contains information identifying the plurality of concatenated time slots* (memory or storing section in Figs. 2-3; For example see Col. 14, Lines 1-29; Col. 15, Lines 13-32)

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of *the memory coupled to the pointer determining circuit contains information identifying the plurality of concatenated time slots* by using the storing section in combination with the pointer processing section as taught by **Fukunaga** in **Helton**'s system with the motivation being to improve the ability to concatenate the data signal in SONET system.

- Regarding claims 4, 7 and 20-21, **Helton** further discloses *the plurality of time slots are grouped in frames including N time slots, where N is an integer,* (For example see details in Fig.

3), *the memory comprises a first submemory* (active half of the data memory or routing memory) *having N storage locations, selected storage locations in the first memory being configured to store identification information associated with the first one of the plurality of the time slots in sequence* (For example see details in Figs. 2-4; Col. 2, Line 64 through Col. 3, Lines 25; Col. 3, Line 60 through Col. 4, Line 20) *and a second submemory* (standby half of the data memory or routing memory) *having N storage locations, selected storage locations in the second memory being configured to store identification information associated with subsequent ones of the plurality of the time slots following the first one in the sequence* (For example see details in Figs. 2-4; Col. 2, Line 64 through Col. 3, Lines 25; Col. 3, Line 60 through Col. 4, Line 20), but fails to disclose about *the concatenated time slots in sequence.* However, such implementation is known in the art.

For example, **Fukunaga** discloses about *the concatenated time slots in sequence* (For example see Col. 14, Lines 1-38; wherein the concatenated data signal multiplexes in TDM)

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of about *the concatenated time slots in sequence* by using the storing section in combination with the pointer processing section as taught by **Fukunaga** in **Helton**'s system with the motivation being to improve the ability to concatenate the data signal in SONET system.

- In regard to claim 5, **Helton** further discloses *the switch circuit comprises a first switch stage* (switching units 101-103 in Fig. 1; For example see Col. 2, Lines 42-63) *coupled to the input circuit* (input optical interfaces 111-113 in Fig. 1) *and a second switch stage* (switching

units 104-106 in Fig. 1; For example see Col. 2, Lines 42-63) *coupled to the output circuit* (output optical interfaces 116-118 in Fig. 1).

- Regarding claims 6 and 8-9, **Helton** further fails to disclose *the additional pointer determining circuit and memory configured to determine the pointer identification within each of the plurality of concatenated time slots in accordance with the pointer identification.* However, such implementation is known in the art.

For example, **Fukunaga** discloses *the additional pointer determining circuit* (concatenation detection section in combination with the pointer value updating section detect the concatenation indication and update the pointer for outputting as disclosed in details of Figs. 30-33) *and additional memory* (RAM 41-44 of the storing section 6-1 in Figs. 9A-B; For example see Col. 14, Lines 1-38; Col. 25, Line 9 through Col. 28, Line 16) *configured to determine the pointer identification* (concatenation indication) *within each of the plurality of concatenated time slots in accordance with the pointer identification.*

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of *the additional pointer determining circuit and memory configured to determine the pointer identification within each of the plurality of concatenated time slots in accordance with the pointer identification* by using the concatenation detection section in combination with the pointer value updating section as taught by **Fukunaga** in **Helton**'s system with the motivation being to improve the ability to concatenate data signal in SONET system.

- In regard to claims 10-12 and 18-19, **Helton** further fails to disclose *the plurality of concatenated time slots constitute at OC-3c or OC-12 and optical signals are transmitted at an OC-48 rate.* However, such implementation is known in the art.

For example, **Fukunaga** discloses *the plurality of concatenated time slots constitute at OC-3c or OC-12* (STS-1/3c/12c; For example see Col. 3, Lines 16-26; Col. 7, Lines 37-46) *and optical signals are transmitted at an OC-48 rate* (STS-N where N=48,192,...; For example see Col. 4, Lines 5-10).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of *the plurality of concatenated time slots constitute at OC-3c or OC-12 and optical signals are transmitted at an OC-48 rate* by using pointer processing in different environment as taught by **Fukunaga** in **Helton**'s system with the motivation being to improve the ability to improve the transmission data signal in SONET system.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Diaz et al. (U.S.5,361,255), **Haas** (U.S.5,485,298), **Yoshifuji et al.** (U.S.5,537,405), **Engbersen et al.** (U.S.6,058,119), **De Moer et al.** (U.S.6,147,968) and **Parruck et al.** (U.S.5,257,261) are all cited to show devices and methods for improving the data transmission of SONET system, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan whose telephone number is (703) 305-7444. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Olms can be reached on (703) 305-4703.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-3900.

Tri H. Phan
January 31, 2003